

Low Temperature Cofired Ceramic: An enabler of high power RF integrated amplifiers

Pierre-Marie Piel, John Estes, Scott Marshall, Garry Funk and Anthony Pavio
Motorola, Tempe AZ 85284

ABSTRACT — Multi-layer ceramic technologies have been viewed recently as an enabler to increase the electrical functionality in a cost effective manner for high power discrete transistors. High power applications have stringent requirements on conductor losses, thermal characteristics and repeatability of design. We present a characterization of these factors and a preliminary definition of the boundary conditions for use in RF amplifiers.

I. INTRODUCTION

Low temperature co-fired ceramics (LTCC) has seen wide spread use in wireless applications, such as filters, VCOs, switches and RF modules, due to its low dielectric loss tangent, good metal conductivity and high component integration capability [1,2]. While LTCC has been used primarily in low voltage, low power devices to date, its properties also provide benefits at higher RF powers and consequently a greater effort is being put forth in developing high powered LTCC applications [3].

One area where LTCC can make an impact at high power is the integration of impedance matching networks for high power (in excess of 100 watts) packaged RF amplifiers. Currently, MOS capacitors and wire bond inductors are used as matching elements in high powered PA packages, but require a complex and expensive manufacturing process. Embedding these components in LTCC has the potential to significantly reduce the cost and number of manufacturing steps.

Using LTCC in an application where low impedances, wide RF feed structures and high current densities are present, raises challenges, which are typically not encountered in low power devices. Since wide RF feed structures (100-200 mils) are common, due to the wide periphery of the transistor die, and since the transistor needs to be matched to extremely low impedances, measuring these matching networks outside the PA package requires complex test and measurement fixtures. Therefore, accurate modeling is needed and repeatability of LTCC substrates is required. Additionally, circuitry in the LTCC substrate will see large currents and with the drive for higher integration and therefore smaller line definitions, thermal and current handling capabilities need to be addressed.

II. LTCC ELECTRICAL MODELING AND REPEATABILITY

A. Modeling

The modeling of LTCC structures requires the calibration and use of a full wave EM simulator. The first step in qualifying a simulation tool usually involves the development of a simple set of structures such as transmission lines, inductors and capacitors. Their electrical characterization will allow the designers to accurately define the ceramic substrate in terms of the simulator significant parameters (dielectric constant, ceramic and metal layer thickness, and conductor and dielectric losses mainly). Although slightly more difficult to calibrate, 2.5D EM simulators are usually preferred due to their faster computational time. The results that we present were obtained using a commercial 2.5D simulator.

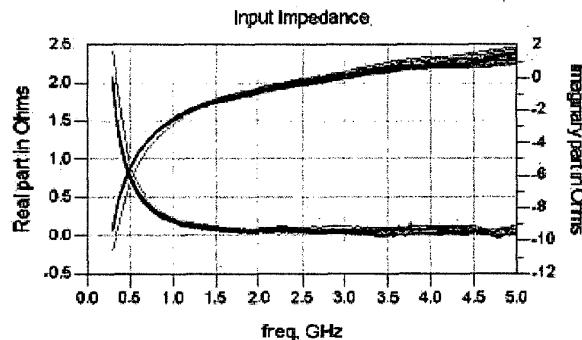


Fig. 1. Comparison of measurement vs. simulation, Capacitor

Figure 1 shows a comparison between the simulation and the measurement for a 45pF capacitor. For this large capacitor, looking comparing the simulated and the measured two ports S-parameters in a 50 Ohms system, does not necessarily give a good idea of the relative agreement, since the reflection is extremely high. In Figure 1, we present the results in terms of the input impedance at port one. The measurements were taken on 21 samples taken from three independently processed ceramic wafers.

The measurements are represented by the black curves and the simulation by the red and blue curves for the real and imaginary parts respectively.

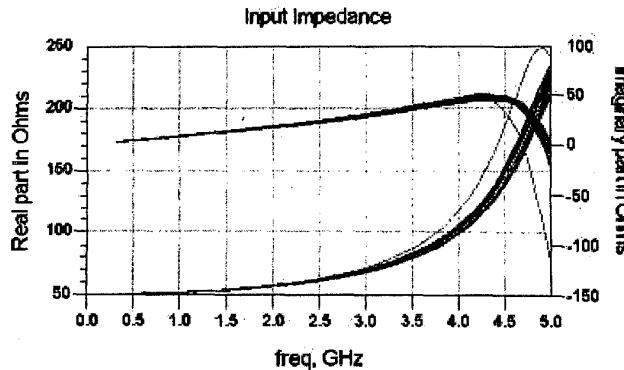


Fig. 2. Comparison of measurement vs. simulation, inductor

Figure 2 shows a comparison between the simulation and the measurement for a 1.8nH inductor. In both cases simulations and measurements show good agreement, especially below 3.5 GHz, which corresponds to our frequency band of interest.

B. Repeatability

The repeatability of the multilayer RF circuit performance is a crucial element for high volume production. We studied several elements that correspond to elementary components such as inductors and capacitors. Table I summarizes our findings for two types of multilayer capacitors, while Table II focuses on inductors. They were all built on the same LTCC/Conductor loading stack-up. The average value (m) was extracted over three lots that were processed at different times, and with other ceramic wafers being processed on the same production line in between the builds. This study thus reflects the variability

TABLE I
REPEATABILITY FOR TWO TYPES OF CAPACITORS

Type		C (1MHz) (pF)	Tol. (%)	Extracted C (pF)	Tol. (%)
45pF	m	44.6	2.7	45.96	2.5
	s	0.4		0.38	
5.5pF	m	5.7	4.21	5.48	4.4
	s	0.08		0.38	

one can expect in a medium to large-scale production environment.

The value of the capacitance that we present in Table I was extracted from the measured S-parameter using an equivalent lumped element circuit, whose components can

be expressed in closed form in terms of the Z-parameters. The frequency range of the measurement was 0.3 to 8 GHz, with a 20 MHz step. We looked at the repeatability on different perspectives. First the tolerance on the extracted capacitance is 4.4% for the 5.5pF capacitor and 2.5% for the 45.0pF capacitor. The tolerance (Tol. In tables I and II) is defined as 3 times the standard deviation s , over the average value m . These values are also compared to the values of capacitance that were measured for the same parts on a C meter at 1 MHz. The values are in good agreement. We also looked at the variation of the self-resonance frequency (SR) of the component, and this yielded 2.3% and 1.7% respectively. We carried out the same type of study for a series of inductors. The results are summarized in table II, and depict higher tolerance values than for the capacitors. However all the tolerance values are within 6.0 %, which appears acceptable for our purpose.

III.THERMAL AND CURRENT HANDLING

In order to test the current handling capabilities of LTCC for high power RF applications, test coupons were built to verify performance under both DC and RF conditions. Each of the three coupons consisted of a 50 ohm buried microstrip line with line widths of 4, 8.4 and 12.8 mils. The average fired thickness of the metal was 0.73 mils. A minimum coupon thickness was required to allow connector mounting, this necessitated the addition of a raised ground plane that consisted of a set of layers surrounding a matrix of 8 mil diameter thermal via with an 80 mil spacing (Refer Fig. 3).

TABLE II
REPEATABILITY FOR TWO TYPES OF INDUCTORS

Type		Extracted inductance (nH)	Tol. (%)
1.8nH	m	1.81	5.0
	s	0.03	
2.5nH	m	2.49	6.0
	s	0.05	

Each coupon was mounted on a heatsink which housed a thermocouple that recorded the bottom temperature of the coupon. An IR thermal scan of the topside of the coupon was used to monitor the surface temperature, T_1 (refer Fig. 4).

In order to predict the surface temperature of the microstrip conductor it is necessary to determine the heat generated, $Q_i = K_i * A_i * (T_2 - T_1) / H_i$. A parallel plate solution with appropriate thermal spreading resistance was chosen to determine the effective area of the microstrip region, $A_i = [2 * (H_i * 1.3 - 0.7) + W_i] * \text{Length}$. This approximation was derived from the measured data and is very linear over the range of heights investigated (3 to 11 mils). A more useful expression for the LTCC designer is to relate the heat generated to the current carried by the conductor, $Q = I^2 * R_s * (1 + T_R * (T_1 - T_{amb})) * \text{Length} / W_i$, where: R_s = Sheet resistivity of the conductor = 0.0012 Ω/square (0.8 mil print), T_R = Temperature coefficient of resistivity = 0.00038 / $^{\circ}\text{C}$, and T_{amb} = Ambient temperature = 25 $^{\circ}\text{C}$.

The thermal resistance associated with the raised ground plane, $R_{T2} = H_2 / (K_2 * A_2)$, was de-embedded based on the two material's thermal conductivities and geometry. The amalgamate thermal conductivity is: $K_2 = K_C * (1 - A_s / A_T) + K_s * (A_s / A_T) = 4.6 \text{ W/m}^{\circ}\text{C}$, where: K_C = thermal conductivity of ceramic = 3 $\text{W/m}^{\circ}\text{C}$, K_s = thermal conductivity of silver via = 410 $\text{W/m}^{\circ}\text{C}$, and A_s / A_T = ratio of silver via area to total ground plane area.

Finally, the surface temperature of the conductor can be derived from the thermal resistance, $R_{T1} = H_1 / (K_1 * A_1)$, where K_1 = thermal conductivity of ceramic = 3 $\text{W/m}^{\circ}\text{C}$ and preceding equations.

Measured results, hand calculations and simulated results (at 2 and 4 A) are presented in Figure 5 and show excellent agreement.

RF testing at 1.4 and 2.2 GHz is shown in Figure 6. The measured sheet resistance, R_s , was accurately measured at DC, and the values resulting from skin effect were derived to be 0.001735 Ω/square at 1.4 GHz and 0.0029 Ω/square at 2.2 GHz.

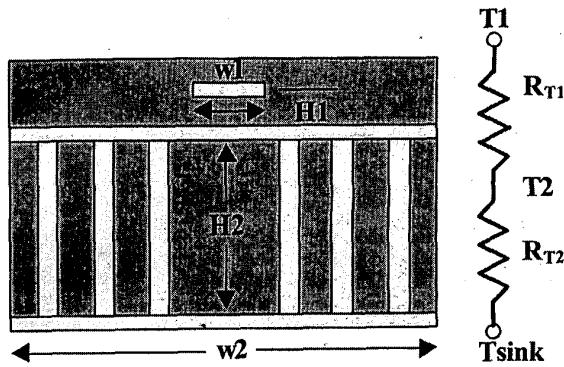


Fig. 3. Cross sectional view of microstrip test coupon. For $w_1=4$ mils, $H_1 = 3.1$ mils and $H_2 = 59.2$ mils. For $w_1=8.4$ mils, $H_1 = 6.8$ mils and $H_2 = 55.5$ mils. For $w_1=12.8$ mils, $H_1 = 10.5$ mils and $H_2 = 51.8$ mils. $W_2 = 480$ mils.

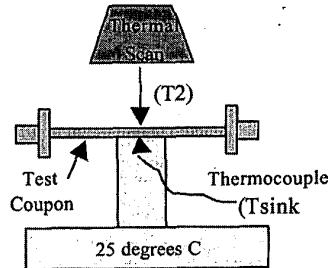


Fig. 4. Measurement setup for acquiring surface temperature of the microstrip transmission lines under DC and RF power conditions. Power was sourced and terminated through SMA connectors.

V. CONCLUSION

This paper has demonstrated that the ability to model structures using a 2.5D EM simulator has been verified using two port measurements. The repeatability of matching structures for use in RF amplifier integration has been characterized at a maximum $3^*s/m$ value of 6%. Thermal and current handling tests have demonstrated that temperatures less than 150 °C can be maintained by using line widths that are 10 mils or greater.

Within the scope of this investigation the potential issues of repeatability, current handling and temperature have not proven to present a limitation to the goal of using LTCC technology in high power discrete RF amplifiers products.

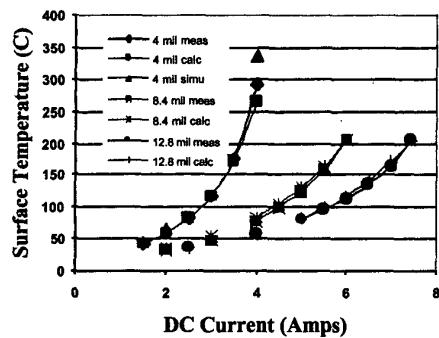


Fig. 5. Surface temperature versus applied DC current for 4, 8.4 and 12.8 mil LTCC microstrip transmission lines and comparison with calculated and measured results.

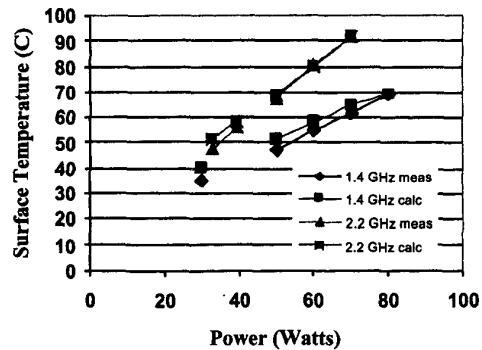


Fig. 6. Surface temperature of a 4 mil microstrip transmission line versus RF power at 1.4 and 2.2 GHz. Comparison of calculated and measured results are shown.

ACKNOWLEDGEMENT

The authors wish to thank Eddie Mares, Peter Vo, Jon Bost and Chia-Yu Fu for their support in this work.

REFERENCES

- [1] Rodolfo Lucero, W. Qutteneh, A. Pavio, D. Meyers, and J. Estes, "Design of an LTCC Diplexer Front-End Module for GSM/DCS/PCS Applications," *2001 IEEE MTT-S Int. Microwave Symposium*
- [2] John Estes, R. Kommrusch, and R.F. Huang, "Integration of a Receiver Front-End in Multilayer Ceramic Integrated Circuit (MCIC) Technology," *1997 IEEE Wireless Communications Conference Proceedings*, pp. 165-169 August 11-13, 1997
- [3] John Estes, P. Piel, G. Shapiro, A. Pavio, M. Hurst, J. Call, and G. Funk, "An Internally Matched LTCC 3G WCDMA 180 Watt LDMOS Power Amplifier," *2001 IEEE MTT-S Int. Microwave Symposium*